

WHAT IS CLAIMED IS:

- 1 1. An apparatus comprising:
 - 2 an interface; and
 - 3 a cache coupled to the interface, wherein the cache is configured to transmit an
 - 4 address of a cache block to be evicted from the cache on the interface, and wherein the
 - 5 cache includes a memory configured to store a plurality of cache blocks including the
 - 6 cache block, and wherein the memory is coupled to receive the address from the
 - 7 interface, and wherein the memory is configured to access the cache block in response to
 - 8 the address for transmission on the interface.
- 1 2. The apparatus as recited in claim 1 wherein the cache is further configured to transmit
- 2 the cache block on the interface.
- 1 3. The apparatus as recited in claim 1 wherein the cache includes an input path, and
- 2 wherein a read address received from the interface traverses the input path to access the
- 3 cache, and wherein the same input path is traversed by the address to access the cache
- 4 block.
- 1 4. The apparatus as recited in claim 1 further comprising a tag memory coupled to
- 2 receive a second address from the interface and configured to output a plurality of tags
- 3 corresponding to cache storage locations eligible to store a second cache block addressed
- 4 by the second address, wherein the cache is configured to select a first cache storage
- 5 location of the cache storage locations to store the second cache block if the second
- 6 address is a miss in the cache, and wherein the address of the cache block comprises a
- 7 first tag of the plurality of tags, the first tag corresponding to the first cache storage
- 8 location.
- 1 5. The apparatus as recited in claim 4 further comprising a plurality of comparators, each
- 2 of the plurality of comparators coupled to receive a respective one of the plurality of tags
- 3 and a tag portion of the second address, and wherein the plurality of comparators are
- 4 configured to compare the plurality of tags to the tag portion of the second address to

- 5 detect the miss.
- 1 6. The apparatus as recited in claim 1 further comprising a data buffer coupled to the
2 memory, wherein the data buffer is configured to store the cache block read from the
3 memory for transmission on the interface.
- 1 7. The apparatus as recited in claim 1 wherein the interface is a bus.
- 1 8. The apparatus as recited in claim 1 wherein the cache transmits the address on the
2 interface as a write transaction.
- 1 9. A cache comprising:
2 a memory configured to store a plurality of cache blocks; and
3 a control circuit configured to transmit an address of a cache block to be evicted
4 from the cache on an interface to which the cache is couplable;
5 wherein the memory is coupled to receive the address from the interface and is
6 configured to access the cache block in response to the address for transmission on the
7 interface.
- 1 10. The cache as recited in claim 9 wherein the control circuit is configured to detect a
2 miss in the cache and to select the cache block from the plurality of cache blocks in
3 response to detecting the miss.
- 1 11. The cache as recited in claim 10 further comprising a tag memory coupled to receive
2 a second address from the interface and configured to output a plurality of tags
3 corresponding to cache storage locations eligible to store a second cache block addressed
4 by the second address, wherein the control circuit is configured to select a first cache
5 storage location of the cache storage locations to store the second cache block if the
6 second address is a miss in the cache, and wherein the address of the cache block
7 comprises a first tag of the plurality of tags, the first tag corresponding to the first cache
8 storage location.
- 1 12. The cache as recited in claim 11 further comprising a plurality of comparators, each
2 of the plurality of comparators coupled to receive a respective one of the plurality of tags

3 and a tag portion of the second address, and wherein the plurality of comparators are
4 configured to compare the plurality of tags to the tag portion of the second address and
5 are coupled to provide an indication of the comparison to the control circuit.

1 13. The cache as recited in claim 9 further comprising an input path for addresses
2 received from the interface, wherein the same input path is used for the address of the
3 cache block.

1 14. The cache as recited in claim 9 further comprising a data buffer coupled to the
2 memory, wherein the data buffer is configured to store the cache block read from the
3 memory for transmission on the interface.

1 15. The cache as recited in claim 9 wherein the address is part of a write transaction on
2 the interface.

1 16. A method comprising:

2 a cache transmitting an address of a cache block to be evicted from the cache on
3 an interface; and

4 in response to the transmitting, reading the cache block from a data memory of the
5 cache for transmission on the interface.

1 17. The method as recited in claim 16 further comprising transmitting the cache block on
2 the interface.

1 18. The method as recited in claim 16 further comprising:

2 detecting a miss of a second address in the cache; and

3 selecting the cache block for eviction responsive to the detecting.

1 19. The method as recited in claim 16 wherein the transmitting is part of a write
2 transaction.

1 20. The method as recited in claim 16 further comprising storing the cache block in a
2 data buffer responsive to the reading.